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(54) Amplifier with reduced input capacitance

(57) A JFET preamplifier for use with a high impedance transducer, having an inherently capacitive input bias impedance. The capacitance of the input bias impedance is effectively neutralized by capacitively coupling the JFET gate bias circuit to the source electrode of the JFET. The JFET preamplifier is configured as a source follower which reduces any capacitance between the JFET gate and source electrode by the open loop gain of the amplifier. By capacitively coupling the JFET gate bias circuit capacitance to the JFET source electrode, the overall input capacitance of the preamplifier stage is reduced.

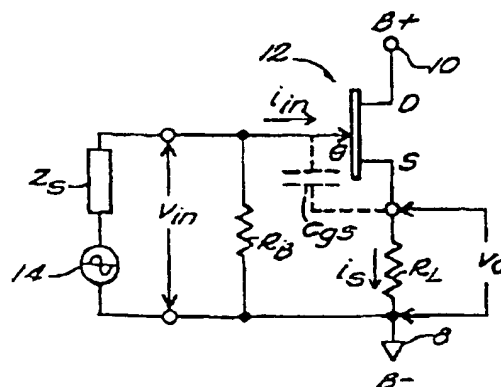


FIG. 1
(PRIOR ART)



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EUROPEAN SEARCH REPORT

Application Number
EP 98 10 8001

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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			H03F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 5 December 2000	Examiner Tyberghien, G
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 98 10 8001

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